Amendment to Claims

This listing of Claims will replace all prior versions and listings of claims in this Application.

Listing of Claims

Claim 1. (CURRENTLY AMENDED) A method of forming an H_2 passivation layer in an FeRAM, comprising:

preparing a silicon substrate, including doping to form a P-type silicon wafer, including threshold adjustment ion implantation, shallow trench isolation ~~to form trenches and filling of the trenches so formed with oxide~~, growth of a gate oxide, deposition of a polysilicon layer, ion implantation to form an N^+ source and an drain; smoothing the oxide by CMP, and patterning and etching the polysilicon layer;

depositing a layer of TiO_x thin film, where $0<x<2$, on a damascene structure;

plasma space etching of the TiO_x thin film to form a TiO_x sidewall;

annealing the TiO_x side wall thin film to form a TiO_2 thin film;

depositing a layer of ferroelectric material; and

metallizing to form a FeRAM.

Claim 2. (ORIGINAL) The method of claim 1 wherein said plasma space etching precedes said annealing.

Claim 3. (ORIGINAL) The method of claim 1 wherein said annealing precedes said plasma space etching.

Claim 4. CANCELLED

Claim 5. (CURRENTLY AMENDED) The method of claim 1 which includes, after said preparing, depositing a layer of oxide; smoothing the oxide by CMP, stopping at the level of the polysilicon layer; depositing a bottom electrode; depositing another layer of oxide by CVD; ~~and~~ smoothing the other layer of oxide by CMP, stopping said smoothing at the level of the bottom electrode; depositing yet another layer of oxide by CVD; and patterning and etching ~~both of~~ the oxide layers to form trench structures.

Claim 6. (ORIGINAL) The method of claim 1 wherein said plasma space etching of the TiO_x thin film includes setting TCP RF power at about 370W, setting the bias power to about 130 W at a chamber pressure of about 5 torr; and using etching including BCl_3 at a flow rate of about 30 sccm and Cl_2 at a flow rate of about 58 sccm.

Claim 7. (ORIGINAL) The method of claim 1 wherein said depositing a layer of TiO_x thin film, where $0<x<2$, includes preparing a MOCVD precursor, including dissolving about 0.2 mol $Ti(OC_3H_7)_4$ in Octane, resulting in a precursor solution having a concentration of 0.2 mol $Ti(OC_3H_7)_4$.

Claim 8. (ORIGINAL) The method of claim 7 which further includes injecting the precursor solution into a CVD chamber vaporizer at temperature in the range of between about 80°C to 120°C by a liquid controller at a rate of between about 0.1 ml/min to 0.5 ml/min to form a

precursor gases; maintaining a CVD chamber feed line at a temperature of between about 80°C to 120°C; maintaining the deposition temperature at between about 380°C to 420°C; maintaining the deposition pressure at between about 0.5 torr to 5 torr, and continuing the deposition process for between about five minutes to thirty minutes.

Claim 9. (PREVIOUSLY AMENDED) A method of forming an H_2 passivation layer in an FeRAM, comprising:

preparing a silicon substrate;

depositing a layer of TiO_x thin film, where $0<x<2$, on a damascene structure;

plasma space etching of the TiO_x thin film to form a TiO_x sidewall, including setting TCP Rf power at about 370W, setting the bias power to about 130 W at a chamber pressure of about 5 torr; and using etching including BCl_3 at a flow rate of about 30 sccm and Cl_2 at a flow rate of about 58 sccm;

annealing the TiO_x side wall thin film to form a TiO_2 thin film;

depositing a layer of ferroelectric material; and

metallizing to form a FeRAM.

Claim 10. (CURRENTLY AMENDED) The method of claim 9 wherein said preparing a silicon substrate includes doping to form a P-type silicon wafer, including threshold adjustment ion implantation, shallow trench isolation ~~to form trenches and filling of the trenches so formed with oxide~~, growth of a gate oxide, deposition of a polysilicon layer, ion implantation to form an N^+ source and an drain; smoothing the oxide by CMP, and patterning and etching the polysilicon

layer.

Claim 11. (CURRENTLY AMENDED) The method of claim 10 which includes, after said preparing, depositing a layer of oxide; smoothing the oxide by CMP;; stopping at the level of the polysilicon layer; depositing a ~~larger size~~ bottom electrode; depositing another layer of oxide by CVD; and smoothing the other layer of oxide by CMP, stopping said smoothing at the level of the bottom electrode; depositing yet another layer of oxide by CVD; and patterning and etching ~~both~~ of the oxide layers to form trench structures.

Claim 12. CANCELLED

Claim 13. (ORIGINAL) The method of claim 9 wherein said depositing a layer of TiO_x thin film, where $0<x<2$, includes preparing a MOCVD precursor, including dissolving about 0.2 mol $Ti(OC_3H_7)_4$ in Octane, resulting in a precursor solution having a concentration of 0.2 mol $Ti(OC_3H_7)_4$.

Claim 14. (ORIGINAL) The method of claim 13 which further includes injecting the precursor solution into a CVD chamber vaporizer at temperature in the range of between about 80°C to 120°C by a liquid controller at a rate of between about 0.1 ml/min to 0.5 ml/min to form a precursor gases; maintaining a CVD chamber feed line at a temperature of between about 80°C to 120°C; maintaining the deposition temperature at between about 380°C to 420°C; maintaining the deposition pressure at between about 0.5 torr to 5 torr, and continuing the deposition process for

between about five minutes to thirty minutes.

Claim 15. (PREVIOUSLY AMENDED) A method of forming an H_2 passivation layer in an FeRAM, comprising:

preparing a silicon substrate;

depositing a layer of TiO_x thin film, where $0<x<2$, on a damascene structure, including preparing a MOCVD precursor, including dissolving about 0.2 mol $Ti(OC_3H_7)_4$ in Octane, resulting in a precursor solution having a concentration of 0.2 mol $Ti(OC_3H_7)_4$;

annealing the TiO_x side wall thin film to form a TiO_2 thin film;

plasma space etching of the TiO_2 thin film to form a TiO_2 sidewall;

depositing a layer of ferroelectric material; and

metallizing to form a FeRAM.

Claim 16. (CURRENTLY AMENDED) The method of claim 15 wherein said preparing a silicon substrate includes doping to form a P-type silicon wafer, including threshold adjustment ion implantation, shallow trench isolation ~~to form trenches and filling of the trenches so formed with oxide~~, growth of a gate oxide, deposition of a polysilicon layer, ion implantation to form an N^+ source and an drain; smoothing the oxide by CMP, and patterning and etching the polysilicon layer.

Claim 17. (CURRENTLY AMENDED) The method of claim 16 which includes, after said preparing, depositing a layer of oxide; smoothing the oxide by CMP;; stopping at the level of the

polysilicon layer; depositing a ~~larger size~~ bottom electrode; depositing another layer of oxide by CVD; ~~and~~ smoothing the other layer of oxide by CMP, stopping said smoothing at the level of the bottom electrode; depositing yet another layer of oxide by CVD; and patterning and etching ~~both~~ of the oxide layers to form trench structures.

Claim 18. (ORIGINAL) The method of claim 15 wherein said plasma space etching of the TiO_x thin film includes setting TCP RF power at about 370W, setting the bias power to about 130 W at a chamber pressure of about 5 torr; and using etching including BCl_3 at a flow rate of about 30 sccm and Cl_2 at a flow rate of about 58 sccm.

Claim 19. CANCELLED

Claim 20. (CURRENTLY AMENDED) The method of claim ~~20~~ 15 which further includes injecting the precursor solution into a CVD chamber vaporizer at temperature in the range of between about 80°C to 120°C by a liquid controller at a rate of between about 0.1 ml/min to 0.5 ml/min to form a precursor gases; maintaining a CVD chamber feed line at a temperature of between about 80°C to 120°C; maintaining the deposition temperature at between about 380°C to 420°C; maintaining the deposition pressure at between about 0.5 torr to 5 torr, and continuing the deposition process for between about five minutes to thirty minutes.